Form PTO-1449 (modified)	Attorney Docket No. 2207/11239	Serial No. 09/895,526
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT(S)' INFORMATION DISCLOSURE STATEMENT	Applicant Yatin HOSKOTE, et al.	
COPY OF PAPERS ORIGINALLY FILED	Filing Date June 29, 2001	Group Art Unit 2121

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*

* - If pertinent

OTHER DOCUMENTS

EXAMINER INITIAL	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
MM	A. Beaumont-Smith, et al., "Reduced Latency IEEE Floating-Point Standard Adder Architectures" IEEE, 1999
	Erdem Hokenek, et al., "Second-Generation RISC Floating Point with Multiply-Add Fused", IEEE Journal of Solid-State Circuits, Vol. 25, No. 5, October 1990, pp 1207-1213
	Fayez Elguibaly, "A Fast Parallel Multiplier-Accumulator Using the Modified Booth Algorithm", IEEE Transactions on Circuits and Systems -- II: Analog and Digital Signal Processing, Vol. 47, No. 9, September 2000, pp 902-908.
	G. Panneerselvam and B. Nowrouzian, "Multiply-Add Fused RISC Architectures for DSP Applications", IEEE Pac Rim '93, pp 108-111
✓	Zhen Luo and Margaret Martonosi, "Accelerating Pipelined Integer and Floating-Point Accumulations in Configurable Hardware with Delayed Addition Techniques" IEEE Transactions on Computers, Vol. 49, No. 3, March 2000, pp 208-218

EXAMINER MM	DATE CONSIDERED 1/1/2004

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.